WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a source and drain formed in a semiconductor substrate;

a crystallized gate insulating film formed on the semiconductor substrate in a region between said source and drain;

a gate electrode formed on said gate insulating film; and

an insulating film formed on a side surface of said gate electrode and having an amorphous structure formed from the same material as that of said gate insulating film.

2. A semiconductor device according to claim 1, wherein said gate insulating film and said insulating film are essentially formed from a material selected from the group consisting of cerium oxide (CeO_2), zirconium oxide (ZrO_2), hafnium oxide (HfO_2), thorium oxide (ThO_2), yttrium oxide (Y_2O_3), calcium fluoride (CaF_2), tin-calcium fluoride ($CaSnF_2$), titanium-barium oxide ($BaTiO_3$), and La_2O_3.

3. A method of manufacturing a semiconductor device, comprising the steps of:

forming a disposable gate on a semiconductor substrate in a region where a gate electrode is to be formed;

forming a sidewall spacer on a sidewall of the

disposable gate;

forming a source and drain in the semiconductor substrate using the disposable gate and the sidewall spacer as a mask;

forming an interlevel insulating film on the semiconductor substrate so as to cover the disposable gate;

planarizing an upper surface of said interlevel insulating film to expose upper surfaces of the disposable gate and the sidewall spacer;

removing the disposable gate to form a trench portion having a side surface formed from the sidewall spacer and a bottom surface formed from the semiconductor substrate;

depositing a gate insulating film on the semiconductor substrate so as to cover the bottom surface and side surface of the trench portion;

forming a gate electrode buried in the trench portion; and

removing the sidewall spacer and said gate insulating film on the sidewall of said gate electrode.

4. A method according to claim 3, further comprising burying a low-dielectric constant insulating film having a dielectric constant lower than that of a thermal oxide film of silicon in a trench formed by removing the sidewall spacer and said gate insulating film on the sidewall of said gate electrode.

5. A method according to claim 4, wherein said low-dielectric constant insulating film is essentially formed from a material selected from the group consisting of SiO_2, SiOF, Fluorinated Amorphous Carbon, Parylene F, Parylene N, Polynaphthalene, Hydrogen Silsesquioxane, Spin-On-Glass, Aerogel/Xerogel, Fluorinated Polyimide, Teflon, Benzocycrobutene, Polyaryl Ether, Fluorinated Polyaryl Ether, and Air gap.

6. A method of manufacturing a semiconductor device, comprising the steps of:

forming a disposable gate on a semiconductor substrate in a region where a gate electrode is to be formed;

forming a sidewall spacer on a sidewall of the disposable gate;

forming a source and drain in the semiconductor substrate using the disposable gate and the sidewall spacer as a mask;

forming an interlevel insulating film on the semiconductor substrate so as to cover the disposable gate;

planarizing an upper surface of said interlevel insulating film to expose upper surfaces of the disposable gate and the sidewall spacer;

removing the disposable gate to form a trench portion having a side surface formed from the sidewall spacer and a bottom surface formed from the

semiconductor substrate;

depositing an insulating film having an amorphous structure on the semiconductor substrate so as to cover the semiconductor substrate on the bottom surface of the trench portion;

epitaxially growing an insulating film having a single-crystal structure from said insulating film having the amorphous structure on the bottom surface of the trench portion to form a gate insulating film on the bottom surface of the trench;

depositing a gate electrode material on the semiconductor substrate so as to bury the trench portion; and

removing the gate electrode material on said interlevel insulating film and said insulating film having the amorphous structure to form a gate electrode buried in the trench portion.

7. A method according to claim 6, further comprising, before deposition of the gate electrode material, selectively etching said insulating film having the amorphous structure on the side surface of the trench portion.

8. A method according to claim 7, further comprising, before deposition of the gate electrode material, modifying said insulating film having the amorphous structure on the side surface of the trench portion to form a conductor.

9. A method according to claim 8, wherein

said insulating film is formed from an HfO_2 film, and

said method further comprises nitriding said insulating film to form HfN as the conductor.